<u>S/N 09/069668</u> <u>PATENT</u>

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kie Y. Ahn et al.

Examiner: W. Coleman

Serial No.:

09/069668

Group Art Unit: 2823

Filed:

April 29, 1998

Docket: 303.466US1

Title:

BIPOLAR TRANSISTORS WITH LOW-RESISTANCE EMITTER CONTACTS

## **COMMUNICATION CONCERNING RELATED APPLICATION(S)**

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No. 09/030430 6121126	Filing Date February 25, 1998	Attorney Docket 303.401US1	Title METHODS AND STRUCTURES FOR METAL INTERCONNECTIONS IN INTEGRATED CIRCUITS
09/031637 6492694	February 27, 1998	303.409US1	HIGHLY CONDUCTIVE COMPOSITE POLYSILICON GATE FOR CMOS INTEGRATED CIRCUITS
09/964172 6573169	September 26, 2001	303.409US3	HIGHLY CONDUCTIVE COMPOSITE POLYSILICON GATE FOR CMOS INTEGRATED CIRCUITS
09/030113 6143655	February 25, 1998	303.474US1	METHODS AND STRUCTURES FOR SILVER INTERCONNECTIONS IN INTEGRATED CIRCUITS
09/614492 6541859	July 11, 2000	303.474US2	METHODS AND STRUCTURES FOR SILVER INTERCONNECTIONS IN INTEGRATED CIRCUITS
09/030188 5920121	February 25, 1998	303.475US1	METHODS AND STRUCTURES FOR GOLD INTERCONNECTIONS IN INTEGRATED CIRCUITS

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## COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 09/069668 Filing Date: April 29, 1998

Title: BIPOLAR TRANSISTORS WITH LOW-RESISTANCE EMITTER CONTACTS

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09/188970 6100176 November 10, 1998

303.475US2

METHODS AND STRUCTURES FOR GOLD INTERCONNECTIONS IN INTEGRATED CIRCUITS

Respectfully submitted,

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<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29th day of <u>December</u>, 2003.

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Tirry IVIO

Signature